UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,733	03/31/2004	Van Hoa Lee	AUS920040057US1	7203

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EXAMINER
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ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 10/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	10/814,733	LEE, VAN HOA
	Examiner	Art Unit	
	Yaima Campos	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>02 August 2006</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

   4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

   Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

   Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   a)☐ All b)☐ Some * c)☐ None of:

     1.☐ Certified copies of the priority documents have been received.

     2.☐ Certified copies of the priority documents have been received in Application No. _____.

     3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

   * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
   Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

1.   The examiner acknowledges the applicant's submission of the amendment dated August

2, 2006. At this point claims 1 and 7-20 have been amended and no claims have been cancelled.

Thus, 20 claims are pending in the instant application.

I. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

2.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

3.   **Claims 1-5, 7-13, and 15-20** are rejected under 35 U.S.C. 103(a) as being unpatentable

over Arndt (US 6,877,158) in view of Stine et al. (US 6,629,111).

As per **claims 1, 7, 15 and 20**, Arndt discloses "a method of supporting memory

addresses with holes, the method comprising the computer implemented steps of: virtualizing a

first physical address range allocated for system memory for an operating system run by a

processor configured to support logical partitioning to produce a first logical address range;

virtualizing a second physical address range allocated for system memory for the operating

system to produce a second logical address range, wherein the first physical address range and

the second physical address range are non-contiguous and the first logical address range and the

second logical address range are contiguous" as **["methods and systems for managing**

resources among multiple operating system images within a logically partitioned operating system" (Column 1, lines 1-13) wherein different I/O adapters are assigned to different partitions (Column 3, lines 3-16) and explains having discontinuous physical memory for these continuous logical partitions (Column 5, line 59-Column 6, line 19). Please also note (Columns 9, line 36 – Column 10, line 35)].

Arndt does not disclose expressly "virtualizing a memory mapped input/output physical address range that is intermediate the first physical address range and the second physical address range to produce a third logical address range, wherein a lowermost logical address of the third logical address range exceeds a respective uppermost logical address of the first and second logical address ranges."

Stine discloses "virtualizing a memory mapped input/output physical address range that is intermediate the first physical address range and the second physical address range to produce a third logical address range, wherein a lowermost logical address of the third logical address range exceeds a respective uppermost logical address of the first and second logical address ranges" as ["a memory allocation scheme which may be used to conserve memory that is to be accessed by one or more clients (e.g. computers or applications)" (Column 5, lines 5-8) and explains identifying regions of memory which may normally go unused "memory holes" and allocating these regions to clients (Column 3, lines 8-56, Figure 10 and Column 10, lines 9-51) and explains that "once mapped to a particular file, the entry ma store information associated with that particular file, such as the name of the file, the size of the file, and the hole size defining an unallocated portion of the memory segment once the file

has been stored in the memory segment" (Column 3, line 57-Column 5, line 5) wherein

memory is mapped using a TLB (Column 5, lines 6-24)].

Arndt (US 6,877,158) and Stine et al. (US 6,629,111) are analogous art because they are

from the same field of endeavor of computer memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in

the art modify the logically partitioned virtualization system wherein a non-contiguous physical

address range is virtualized into a contiguous virtual address range as taught by Arndt and map

memory access operations within memory holes as taught by Stine.

The motivation for doing so would have been because Stine discloses that allocating

"memory holes" to processes or applications allows [the conservation of physical memory as

"the corresponding number of pages required in virtual memory are minimized;" also

facilitating the utilization of memory as "when a hole in a memory segment already

containing data is used, a new TLB entry need not be created since the hole is mapped in

an entry in the memory segment list" (Column 4, lines 6-24)]. Furthermore, Arndt discloses

the having a logically partitioned system wherein partitions are assigned to different resources

wherein noncontiguous physical memory is assigned to contiguous virtual partitions is desirable

as it allows ["fine grain allocation of resources to partitions without necessitating the

physical movement of the hardware during configuration" (Column 1, line 66-Column 2,

line 3)].

Therefore, it would have been obvious to combine Stine et al. (US 6,629,111) with Arndt

(US 6,877,158) for the benefit of creating a memory virtualization system to obtain the invention

as specified in claims 1, 7, 15 and 20.

4.   As per **claims 2, 8-11 and 16-19**, the combination of Arndt and Stine discloses the

method/program/system of claims 1, 7 and 15 **[See rejection to claims 1, 7 and 15 above]**

wherein "the steps of virtualizing the first physical address range, the second physical address

range, and the memory mapped input/output physical address range comprises maintaining a

mapping table that defines physical addresses and corresponding logical addresses" **[With**

respect to this limitation, Arndt discloses having a page frame table per OS image wherein

different OS images are assigned to different logical partitions and a "hypervisor 310" for

performing virtualization having "allocation table 380" (Column 5, lines 37-49; Figure 3;

Column 3, lines 3-16). Furthermore, Stine discloses virtualization using a "TLB" (Figure

1B)].

5.   As per **claim 3**, the combination of Arndt and Stine discloses the method program of

claim 2, **[See rejection to claim 2 above]** "wherein maintaining the mapping table further

comprises maintaining the mapping table in a physical address space allocated to one of the first

and second physical address ranges, and wherein the physical address space is unavailable to an

operating system accessing the first and second physical address ranges" **[Arndt discloses this**

concept as a "hypervisor 210" having allocation table 380 which controls platform's 200

virtual address translation hardware 280 (Column 4, line 58-Column 5, line 30; Figures 2-

3)].

6.   As per **claims 4 and 12**, the combination of Arndt and Stine discloses the

method/program of claims 1 and 7," **[See rejection to claims 1 and 7 above]** "wherein the third

logical address range is non-contiguous with the first logical address range and the second

logical address range" **[Arndt discloses this concept as "a different contiguous range of**

virtual address pages of virtual address being associated with each one of the partitions"

(Column 10, lines 5-7). Furthermore, Stine discloses mapping memory holes in existing

TLB entries (Column 4, lines 6-24)].

7.   As per **claim 5 and 13**, the combination of Harvey and Stine discloses "The method of

claim 1," **[See rejection to claim 1 above]** "further comprising: allocating a portion of at least

one of the first physical address range and the second physical address range for a logical

partitioning management software layer" **[With respect to this limitation, Arndt discloses**

mediated address translation system (Column 5, line 39 – Column 6, line 3)].

8.   **Claims 6 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arndt**

(US 6,877,158) in view of Stine et al. (US 6,629,111) as applied to claims 1-5 above, and further

in view of Yazdy et al. (US 6,256,710).

9.   As per **claims 6 and 14**, the combination of Arndt and Stine discloses the

method/program of claims 1 and 7, **[See rejection to claims 1 and 7 above]** but does not

expressly disclose having a "memory mapped input/output physical address range is allocated for

cache inhibited addresses."

Yazdy discloses having a "memory mapped input/output physical address range is

allocated for cache inhibited addresses" as **[a software system in which "it may be desirable in**

certain cases to define areas of main memory as being non-cacheable" and explains

"declaring one or more ranges of memory as non-cacheable" (Figure 1 and Column 2, lines

23-41). Note that figure 1 shows a block of "non-cacheable data" placed between two blocks

of cacheable data as claimed by Applicant].

Arndt (US 6,877,158), Stine et al. (US 6,629,111) and Yazdy et al. (US 6,256,710) are analogous art because they are from the same field of endeavor of computer memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art modify the memory virtualization system which includes a memory gap/hole as taught by Harvey, further map memory access operations within this memory hole as taught by Stine and further use a gap/hole to store cache-inhibited data, as taught by Yazdy.

The motivation for doing so would have been because Yazdy discloses that allocating a memory block for cache-inhibited address ["**by providing software with the opportunity to define its own regions of non-cacheable main memory, cache performance can be optimized by looking to the cache for ranges of main memory which are more likely to be reaccessed" (Column 2, lines 54-58)**].

Therefore, it would have been obvious to combine Yazdy et al. (US 6,256,710), Stine et al. (US 6,629,111) and Arndt (US 6,877,158) for the benefit of creating a memory virtualization system to obtain the invention as specified in claims 6 and 14.

II. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

10.   The following is a summary of the treatment and status of all claims in the application as

recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

11.   Per the instant office action, claims 1-20 have received a second action on the merits and

are subject of a second action non-final.

b. DIRECTION OF FUTURE CORRESPONDENCES

12.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Yaima Campos whose telephone number is (571) 272-1232. The

examiner can normally be reached on Monday to Friday 8:30 AM to 5:00 PM.

IMPORTANT NOTE

13.   If attempts to reach the above noted Examiner by telephone are unsuccessful, the

Examiner's supervisor, Mr. Sanjiv Shah, can be reached at the following telephone number: Area

· Code (571) 272-4098.

        The fax phone number for the organization where this application or proceeding is

assigned is 571-273-8300. Information regarding the status of an application may be obtained

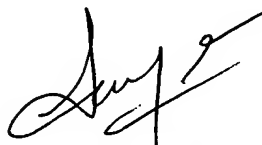from the Patent Application Information Retrieval (PAIR) system. Status information for ·

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on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-

9197 (toll-free).

October 14, 2006

Yaima Campos
Examiner
Art Unit 2185

SANJIV SHAH
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